Pass Transistor Circuits

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Outline

1. Pass Transistor Circuits
2. The CMOS Transmission Gate
3. Design Example
4. Transmission Gate Design Methodology
We can view the complementary CMOS gate as switching the output pin to one of power or ground.
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In such designs the MOSFET is considered to be a pass transistor.

When used as a pass transistor the device may conduct current in either direction.
Pass Transistor Truth Table

\[ \begin{array}{ccc}
A & B & X \\
0 & 0 & Z \\
\end{array} \]
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0 & 0 & Z \\
0 & 1 & 0 \\
\end{array}
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### Pass Transistor Truth Table

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Properties of Pass Transistors

For the n-channel pass transistor circuit note that:

1. “Z” in the truth table implies a floating node.

2. For the n-channel pass transistor, when A = B = 1, the output voltage at X is:

   \[ V_x = \min(\ V_B - V_t, \ V_A) \]

3. This if \( V_A = V_B = 3 \) and \( V_B = 0 \) then \( V_x = 2 \).

4. This reduction in output voltage makes cascading of pass transistor circuits difficult.
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Cascaded Pass Transistors

Figure: Cascaded pass transistors

Vdd

Vdd

Vdd

Vdd

Vdd

Vdd

Vdd - Vt

Vdd - 2Vt

Vdd - 3Vt

Vdd - 2Vt

Vdd - 3Vt

Vdd - Vt

Vdd - 3Vt
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4. Full logic levels can be regenerated with an inverter at the output of the gate.
Two-to-One Mux

Figure: Two-to-one Mux
When $S = 1$ the output $Z$ is connected to $B$
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When $S = 0$ the output $Z$ is connected to $A$
Two-to-One Mux - 2

- When \( S = 1 \) the output \( Z \) is connected to \( B \)
- When \( S = 0 \) the output \( Z \) is connected to \( A \)
- Note that the connection made is *bidirectional*
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![CMOS Transmission Gate Circuit](image)

Figure: CMOS Transmission Gate Circuit

When $C = 1$, A and B are connected, both logic zero and logic one can be transmitted without degradation.
Transmission gates are widely used and shorthand symbols are used.
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```
  C
A -- X -- B
  C
```

- The most commonly used symbol is simply:

```
  A -- B
      C
```
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\[ C \]

\[ \overline{C} \]

\[ \begin{array}{c}
  \text{A} \\
  \text{B} \\
  \text{C}
\end{array} \]

The most commonly used symbol is simply:

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  \text{B} \\
  \text{C}
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A common design technique used with transmission gate structures is the use of multiplexor based architectures. Consider the Boolean function

$$f = A \overline{S}_2 S_1 + B \overline{S}_2 . \overline{S}_1 + 1 . S_2 S_1 + 0 . S_2 S_1$$
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\[ f = A S_2 \overline{S_1} + B \overline{S_2} \overline{S_1} + \overline{S_2} S_1 \]

This may be rewritten as (the reason will become clear later):

\[ f = A S_2 \overline{S_1} + B \overline{S_2} \overline{S_1} + 1 \overline{S_2} S_1 + 0 \overline{S_2} S_1 \]
Transmission Gate Implementation:

Figure: Implementation with Transmission Gates
Note the need for the term $0.S_1S_2$. If not present then when $S_1 = S_2 = 1$ the output $f$ would float.
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4. Where lines connect only to logic 0 the pMOS devices may be omitted.

5. nMOS and pMOS devices may be grouped to minimise the number of wells required.
Transistor Schematic

Figure: Transistor Level Schematic for Design
Design Methodology

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- The output is always driven to logic 1 or logic 0.
- There are no "sneak" paths, such as:
Viable design approaches are:

- Choose a number of inputs as mux select inputs and proceed as above.
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- Plot variables on K-maps.
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- Plot variables on K-maps.
- Tabular methods such as modifications of Quine-McCluskey - not covered here.
Plotting Variables

\[ f = \overline{a} \overline{b} + \overline{b} \overline{c} \overline{d} + acd \]
Plotting Variables

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and we will look for a network using \(d\) and \(\overline{d}\) as inputs. Plotting the function on a K-Map gives:
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Plotting again with $d$ as input

Now plot the K-Map using $d$ as an input, giving:

$$f = \overline{a} \overline{b} + b \overline{c} \overline{d} + ac \overline{d} + \overline{a} \overline{b} \overline{c} + \overline{a} \overline{b} \overline{c} \overline{d}$$
Now plot the K-Map using $d$ as an input, giving:

![K-Map Diagram]

Giving the Boolean expression for $f$ as:

$$f = \overline{a}\overline{b} + b\overline{c}d + a\overline{b}\overline{c}.0 + \overline{a}bc.0$$
Plotting again with d as input

Now plot the K-Map using \( d \) as an input, giving:

\[
\begin{array}{c|cccc}
  & 00 & 01 & 11 & 10 \\
\hline
0 & 1 & d & d & 0 \\
1 & 1 & 0 & d & d \\
\end{array}
\]

Giving the Boolean expression for \( f \) as:

\[
f = 1 \cdot \bar{a}b + b\bar{c}d + ac \cdot d + a\bar{b}\bar{c} \cdot 0 + \bar{a}bc \cdot 0
\]